

**AMENDMENT TO THE CLAIMS:**

This listing of the claims will replace all prior versions, and listings, of claims in the application.

**LISTING OF CLAIMS:**

Claim 1. (Original) An interconnect structure comprising:

a semiconductor substrate comprising one or more device regions; and

one or more interconnect levels located atop the semiconductor substrate, said one or more interconnect levels comprising a patterned organosilicate dielectric having sidewalls, wherein said sidewalls are not substantially altered either chemically or physically.

Claim 2. (Original) The interconnect structure of Claim 1 wherein said patterned organosilicate dielectric has a dielectric constant of less than 4.0.

Claim 3. (Original) The interconnect structure of Claim 1 wherein said one or more interconnect levels include metal lines and vias.

Claim 4. (Original) The interconnect structure of Claim 3 wherein the metal lines and vias comprise a conductive material.

Claim 5. (Original) The interconnect structure of Claim 1 wherein said one or more interconnect levels form a thinwire interconnect structure.

Claim 6. (Currently Amended) The interconnect structure of Claim 1 wherein said one or more interconnect levels form a ~~thinwire~~ fatwire interconnect structure.

Claim 7. (Original) The interconnect structure of Claim 1 wherein said one or more device regions comprise a field effect transistor.

Claims 8-20. (Cancelled)